

REMARKS/ARGUMENTS

Claims 1-13 are pending. Claims 1, 2, and 4-13 have been amended. Claims 1-12 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. One or more claims have been amended in response to the rejection,

Claims 1, 2, 4, 5, and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hobbs et al. Applicants respectfully traverse the rejection. Claim 1 is directed to a semiconductor device having a gate insulation film including titanium oxide and having a low current leakage via the gate insulating film. As described in the Background section, the semiconductor device technology is moving towards smaller and smaller devices. Accordingly, the semiconductor device is provided with a thinner and thinner gate oxide. Such a thin gate oxide, e.g., 2 nm, needs to have a high dielectric constant. Titanium oxide has been identified has a suitable gate oxide of the future due to its high dielectric constant.

However, the problem with the use of titanium oxide is that it is associated with a relatively high current leakage problem due to diffusion of conductive material into the titanium oxide (see page 2, 1st paragraph). Accordingly, implementation of the titanium oxide as the gate oxide has encountered some difficulty.

One of the features of the claim invention is to solve the above current leakage problem associated with the use of titanium oxide. The present inventors have discovered that the use of a gate electrode film including ruthenium oxide or iridium oxide effectively reduces or prevents diffusion of elements into the titanium oxide. That is, the gate electrode film has "a dual function of being an electrode and a diffusion barrier," thereby reducing a current leakage problem associated with the use of titanium oxide in the gate insulation film (see, Figs. 2-9).

On the other hand, Hobbs et al. is directed a semiconductor device having a gate electrode made of metal rather than polysilicon (col. 1, lines 50-63). The use of metal causes problems in adjusting channel threshold voltages since metals cannot be easily doped, unlike polysilicon. Hobbs et al. solves the above problem by using dummy structures 201 and 202 that are subsequently replaced with metal structures (col. 2, lines 50-53; col. 3, lines 47-55).

Accordingly, Hobbs et al. is not directed to solving the current leakage problem associated with the use of titanium oxide as the gate oxide. Although Hobbs recites use of the iridium oxide and ruthenium oxide as the gate electrode, they were merely listed as part of a comprehensive list of suitable metals without any appreciation their effectiveness in serving as diffusion barriers with respect a gate oxide including titanium oxide. In fact, Hobbs does not even appear to appreciate the current leakage problem associated with the use of titanium oxide in the gate oxide.

Therefore, there is no motivation to provide a semiconductor device having a combination of "a gate insulation film formed on one major surface of said semiconductor substrate and including titanium oxide" and a "gate electrode film having a dual function of being an electrode and a diffusion barrier, said gate electrode film being configured to minimize diffusion of conductive elements into said gate insulation film to reduce a current leakage via the gate insulation film, said gate electrode film including ruthenium oxide or iridium oxide." Accordingly, claim 1 is allowable.

Claim 4 recites, "a semiconductor substrate; a gate oxide film formed on one major surface of said semiconductor substrate, said gate oxide film being titanium oxide and having a given crystal structure; and a gate electrode formed over said gate insulation film, said gate electrode including a conductive oxide layer and a metal layer, said conductive oxide layer being provided between said gate oxide film and said metal layer." Hobbs et al. does not disclose "said gate electrode including a conductive oxide layer and a metal layer." Claim 4 is allowable.

Claims 3, 6, 12, and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hobbs et al. in view of Tsunashima et al. Applicants respectfully traverse the rejection. Claims 3 and 6 depend from claims 1 and 4, respectively. Therefore, they are allowable at least for the reasons their independent claims are allowable.

Claim 13 recites, "a semiconductor substrate; a gate insulation structure including a first gate insulation film and a second gate insulation film formed on containing titanium oxide of a given crystal structure; and a gate electrode including a first gate electrode film formed in contact with said second gate insulation film and containing ruthenium oxide or iridium oxide

and a second gate electrode film containing one selected from a group consisting of ruthenium, iridium, platinum, tungsten and molybdenum, wherein said given crystal structure of said titanium oxide and said first gate electrode film configured to inhibit diffusion of an element into said gate insulation structure." Hobbs et al. does not disclose the gate insulation structure having the first and second films in the manner recited nor does it show the gate electrode having the first and second electrode films in the manner recited. Tsunashima et al. does not remedy these deficiencies. Therefore, claim 13 is allowable.

Claims 8, 9, and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hobbs et al. in view of Gilbert et al. Applicants respectfully traverse the rejection.

Claim 8 recites, "a semiconductor substrate; a titanium oxide gate insulation film formed on one major surface of said semiconductor substrate; a gate electrode including conductive oxide film and a metal film, said conductive oxide film being in contact with said gate oxide and configured to serve as a diffusion barrier to prevent diffusion of an element into said titanium oxide to reduce a current leakage via said titanium oxide film; a first capacitor electrode formed on said one major surface of said semiconductor substrate; a capacitor insulation film formed in contact with said first capacitor electrode and exhibiting a high dielectric constant or ferroelectricity; and a second capacitor electrode formed in contact with said capacitor insulation film." Hobbs et al. does not disclose or suggest the gate electrode in the manner recited. Gilbert et al. does not remedy this deficiency. Therefore, claim 8 is allowable.

Claim 10 was rejected under 35 U.S.C. as being unpatentable over the combination of Hobbs et al. and Tsunashima et al. Applicants respectfully traverse the rejection. Claim 10 depends from claim 8 and is allowable at least for this reason.

CONCLUSION

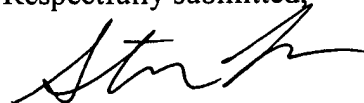
In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Appl. No. 09/943,843
Amdt. dated June 25, 2003
Reply to Office Action of March 27, 2003

PATENT

Respectfully submitted,



Steve Y. Cho
Reg. No. 44,612

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
SYC:syc
PA 3314142 v1